

# Joonwon Choi

PhD Candidate in MIT CSAIL

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## Research Interests

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- ▶ Formal synthesis of protocols in message-passing systems.
- ▶ Formal verification for correct hardware design and synthesis. Take a look at the [Kami](#) project page for details.
- ▶ Formal verification of realistic processors.

## Current Position

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PhD Candidate, MIT CSAIL

Sep 2014 – Present

Advisors: Adam Chlipala and Arvind

## Education

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MIT CSAIL

Sep 2014 – Jun 2016

Master of Science in Electrical Engineering and Computer Science

Seoul National University

Mar 2006 – Feb 2013

Bachelor of Science in Computer Science and Engineering

Double major in Mathematical Sciences

graduated with honors (summa cum laude)

## Publications

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- [1] [Kami: A Platform for High-Level Parametric Hardware Specification and its Modular Verification.](#)  
Joonwon Choi, Muralidaran Vijayaraghavan, Benjamin Sherman, Adam Chlipala, and Arvind.  
Proceedings of the 22nd ACM SIGPLAN International Conference on Functional Programming (ICFP'17).  
September 2017. [[pdf](#)]
- [2] [An Inlining Approach to Formal Hardware Semantics.](#)  
M.S. Thesis in Electrical Engineering and Computer Science. Massachusetts Institute of Technology. [[pdf](#)]  
Thesis Supervisor: Arvind
- [3] [Crellvm: Verified Credible Compilation for LLVM.](#)  
Jeehoon Kang, Yoonseung Kim, Youngju Song, Juneyoung Lee, Sanghoon Park, Mark Dongyeon Shin, Yonghyun Kim, Sungkeun Cho, Joonwon Choi, Chung-Kil Hur, and Kwangkeun Yi.  
To appear in Proceedings of the ACM SIGPLAN 2018 Conference on Programming Language Design and Implementation (PLDI'18). June 2018. [[draft pdf](#)]

## Current Research Projects

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### Formal synthesis of protocols in message-passing systems

- ▶ We are designing a formal synthesis framework, embedded in Coq, for building proven-to-be-correct message-passing systems. The framework provides a way of specifying protocols at a high-level. A synthesizer tries to build an executable implementation that is formally proven to follow the specification. Synthesized implementations may involve a lot of interleavings, where the safety of such interleavings is automatically guaranteed by the synthesis process. As a case study, we are currently trying to synthesize various cache-coherence protocols.

### Formal verification of realistic processors

- ▶ We are designing realistic processors and proving them correct, using the Kami framework. Kami is a Coq framework that supports implementing, specifying, verifying, and compiling Bluespec-style hardware components. Realistic processors are highly optimized in that various components are involved with each others and the components themselves are optimized as well. By using the modular verification framework in Kami, we aim for modular specifications and proofs of such complex processors that naturally follow modular designs.

## Honors & Awards

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Kwanjeong Educational Fellowship	Sep 2014 –	Current
MIT Emerson Scholarship for Private Music Study	Sep 2014 –	Current
Top Honor (summa cum laude) Certification Seoul National University		Feb 2013

## Teaching Experience

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MIT 6.887: Formal Reasoning About Programs Teaching Assistant	Spring 2017
SNU 4190.310: Programming Languages Teaching Assistant	Fall 2013

## Working Experience

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ROSAEC, Korea Research Associate	Mar 2013 – Jul 2014
allm Games, Korea Software Engineer (Skilled Industry Personnel as alternative military service)	Apr 2009 – Oct 2011
Google, Korea Software Engineering Intern (SWE Intern)	Jan 2009 – Apr 2009
SK Communications, Korea Intern (Software Developer)	Jul 2007 – Aug 2007

Last updated: February 13, 2018  
<http://joonwon.net/c/docs/cv.pdf>